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(54) **[Title of the Invention]** Preamplifier Circuit for Photoelectric Conversion

(57) **[Abstract]**

[Object] Relating to a preamplifier circuit for photoelectric conversion used for the input stage or the like of an optical transmitter/receiver in optical telecommunications, the object is to provide a preamplifier circuit that operates stably up to a high transmission bit rate, while ensuring a broad dynamic range.

[Constitution] Formed from a photoelectric conversion element that converts an optical signal into an electric signal, and an inverting amplifier circuit connected to the input terminal and the output terminal, with the converted electric signal as an input signal, and characterized in that said inverting amplifier circuit in constructed in multiple stages, utilizing a plurality of inverting amplifiers, and a variable impedance element is connected to the input terminal and the output terminal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and in addition, there is provided an impedance control means that controls the impedance of said variable impedance element in response to an output signal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and when the input signal increases, the impedance of said variable impedance element is controlled so that it decreases.

EXAMPLE

[Claims of the Invention]

[Claim 1] Preamplifier circuit for photoelectric conversion, formed from a photoelectric conversion element that converts an optical signal into an electric signal, and an inverting amplifier circuit connected to the input terminal and the output terminal, with the converted electric signal as an input signal, and characterized in that said inverting amplifier circuit in constructed in multiple stages, utilizing a plurality of inverting amplifiers, and a variable impedance element is connected to the input terminal and the output terminal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and in addition, there is provided an impedance control means that controls the impedance of said variable impedance element in response to an output signal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and when the input signal increases, the impedance of said variable impedance element is controlled so that it decreases.

[Claim 2] A preamplifier circuit for photoelectric conversion of Claim 1, characterized in that the impedance of the variable impedance element is set so that it is infinitely great at the lowest receiving level for the input signal.

[Claim 3] A preamplifier circuit for photoelectric conversion of Claim 2, characterized in that the variable impedance element is formed from MOS-type FET.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention] The present invention relates to a preamplifier circuit for photoelectric conversion used for the input stage or the like of an optical transmitter/receiver in optical telecommunications.

[0002]

[Prior Art] FIG. 5 shows a prior art preamplifier circuit for photoelectric conversion in an optical transmitter/receiver. In FIG. 5, ***1*** is a photodiode that receives an optical pulse signal and converts it into an input signal current I, ***2*** is an inverting amplifier circuit that amplifies said input signal current I, and ***3*** is a negative feedback resistor that is connected to the input terminal and the output terminal of the inverting amplifier circuit ***2***.

[0003] The preamplifier circuit for photoelectric conversion of FIG. 5 is called a transistor impedance-type preamplifier circuit, and its output voltage V_{OUT} is given by $V_{OUT} = (I \times R_f)$, where R_f is the resistance of the negative feedback resistor ***3***.

[0004] Incidentally, preamplifier circuits for photoelectric conversion that are used in optical telecommunications require a broad dynamic range, since high-speed transmission has to be performed. However, in the case of FIG. 5, when the input signal current I is too large, the output voltage V_{OUT} of the inverting amplifier circuit ***2*** becomes saturated. As a result, the duty ratio of the output pulse changes, so there is the drawback that the dynamic range cannot be broadened.

[0005] Accordingly, heretofore, a method for solving this problem was employed, wherein saturation of the inverting amplifier circuit was prevented by shunting the input signal current to the negative feedback resistor ***3***.

[0006] FIG. 6 shows the circuit structure thereof. In FIG. 6, ***1*** is a photodiode; ***2*** is a multistage inverting amplifier circuit formed from three inverting amplifier circuits 2_1 - 2_3; ***3*** is a negative feedback resistor that is connected to the input terminal and the output terminal of the inverting amplifier circuit ***2***; ***4*** is an N-channel MOS-type FET serving as a variable impedance element for shunting, and is connected to the input terminal and the output terminal of the first-stage inverting amplifier circuit 2_1 of the multistage inverting amplifier circuit; ***5*** is an automatic gain control (AGC) circuit of the main amplifier which is connected to the latter stages of the preamplifier circuit for photoelectric conversion.

[0007] In the case of the preamplifier circuit for photoelectric conversion of FIG. 6, when the input signal current I is amplified and the output voltage V_{OUT} of the inverting amplifier circuit ***2*** increases, the gate voltage of the FET ***4*** is controlled by the AGC circuit ***5*** of the main amplifier of the latter stages, and a portion of the input signal current I is shunted to the FET ***4*** by virtue of the fact that the impedance between the drain (D) and the source (S) of the FET ***4*** is lowered, thereby preventing saturation of the inverting amplifier circuit ***2***.

[0008]

[Problems to Be Solved by The Invention] However, in the case of the preamplifier circuit for photoelectric conversion of FIG. 6, since the FET ***4*** that shunts the input signal current I is controlled by the AGC circuit ***5*** of the main amplifier of the latter stages, there is the drawback that the response speed with respect to changes in the input signal is slow, making it difficult to operate stably up to a high transmission bit rate, while making it difficult to ensure a broad dynamic range.

[0009] The present invention was devised on the basis of the aforementioned situation, and has as its object to provide a preamplifier circuit for photoelectric conversion capable of high-speed response to changes in the input signal, and capable of operating stably up to a high transmission bit rate, while ensuring a broad dynamic range.

[0010]

[Means for Solving These Problems] The present invention is a preamplifier circuit for photoelectric conversion, formed from a photoelectric conversion element that converts an optical signal into an electric signal, and an inverting amplifier circuit connected to the input terminal and the output terminal, with the converted electric signal as an input signal, and characterized in that said inverting amplifier circuit in constructed in multiple stages, utilizing a plurality of inverting amplifiers, and a variable impedance element is connected to the input terminal and the output terminal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and in addition, there is provided an impedance control means that controls the impedance of said variable impedance element in response to an output signal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and when the input signal increases, the impedance of said variable impedance element is controlled so that it decreases.

[0011]

[Operation of the Invention] When the input signal to the inverting amplifier circuit increases, the impedance control means detects this from the changes in the output signal of the first stage inverting amplifier, and controls the impedance of the variable impedance element so that it decreases. Accordingly, a portion of the input signal that enters the negative feedback resistor is shunted to the impedance element side, thereby preventing saturation of the inverting amplifier circuit. Consequently, the duty ratio of the output pulse no longer changes due to saturation of the inverting amplifier circuit.

[0012] Moreover, the response speed with respect to changes in the input signal current is extremely high, and operation is stable up to a high transmission bit rate.

[0013]

[Examples] Examples of the present invention are described with reference to drawings. FIG. 1 depicts an example of a preamplifier circuit for photoelectric conversion of the present invention. In FIG. 1, ***1*** is a photodiode; ***2*** is a multistage inverting amplifier circuit formed from three inverting amplifier circuits $\boldsymbol{2_1}$ - $\boldsymbol{2_3}$; ***3*** is a negative feedback resistor that is connected to the input terminal and the output terminal of the inverting amplifier circuit ***2***; ***4***

is an N-channel MOS-type FET serving as a variable impedance element for shunting, and is connected to the input terminal and the output terminal of the first-stage inverting amplifier circuit ***2_1*** of the multistage inverting amplifier circuit; ***6*** is an impedance control amplifier. It should be noted that the parts that are the same as in the prior art circuit are indicated with the same reference numbers.

[0014] As shown in FIG. 1, the present invention preamplifier circuit for photoelectric conversion is designed in such a way that the impedance control amplifier ***6*** is connected to the output terminal of the first-stage inverting amplifier circuit ***2_1*** of the multistage inverting amplifier circuit, so as to control the gate voltage of the FET ***4*** by this impedance control amplifier ***6***.

[0015] The operation of the circuit of FIG. 1 is explained with reference to FIG. 2 and FIG. 3. It should be noted that FIG. 2 shows the input and output characteristics of the impedance control amplifier ***6***, and FIG. 3 shows the impedance characteristics of the FET ***4***.

[0016] The input signal current I is within a normal operating range that is under the saturation region, and the operating point of the impedance control amplifier ***6*** at this time is given by point ① in FIG. 2, and the corresponding operating point of the FET ***4*** is given by point ② in FIG. 3. Therefore, as shown in FIG. 3, the impedance Z between D and S of the FET ***4*** in this case has a large value on the order of 10 kΩ.

[0017] Now, as the input signal current I increases, and as the current flowing to the FET ***4*** increases, the potential of the input terminal A of the impedance control amplifier ***6*** changes as from point ① to point ② in FIG. 2, and the potential of the output terminal B increases. Accordingly, the operating point of the FET ***4*** changes as from point ① to point ② in FIG. 3, and the impedance Z between D and S of the FET ***4*** drops greatly, from 10 kΩ to 1 kΩ, as shown, for example, in FIG. 3.

[0018] As a result of this drop in impedance, there is an increase in the volume of the input signal current I shunted to the FET ***4***, and there is a decrease in the input signal current I flowing into the negative feedback resistor, and the output voltage V_{OUT} of the inverting amplifier circuit ***2*** is decreased by that amount, thereby preventing saturation of the inverting amplifier circuit ***2*** due to the increase in the input current signal I.

[0019] Therefore, the duty ratio of the output pulse no longer changes due to saturation of the inverting amplifier circuit ***2***. Moreover, since the impedance of the FET ***4*** is controlled using the output signal of the first-stage inverting amplifier circuit ***2_1*** of the multistage inverting amplifier circuit, the response speed with respect to changes in the input signal current is extremely high, and operation is stable up to a high transmission bit rate.

[0020] FIG. 4 shows an example of computed analytic results of output wave forms resulting from the aforementioned example. FIG. 4 shows the analysis of the output pulse wave form of the inverting amplifier *2* when a pulse signal of a transmission bit rate of 28.8 Mbps serves as an input signal, and when the measured value of the current of this input pulse fluctuates. FIG. 4 clearly demonstrates that even if the measured value of the current of the input pulse varies, the rising position and the falling position of the output pulse waveform are almost constant.

[0021] It should be noted that in the aforementioned example, if one sets the output voltage of the impedance control amplifier *6* lower than the gate threshold voltage V_{TH} of the FET *4* when the input signal current I is at the lowest receiving level, it is possible to set the FET *4* at a cut-off state (unlimited impedance) when the input signal current I is at the lowest receiving level, making it possible to eliminate the effect of the thermal noise of the FET *4* when at the lowest receiving level, and making it possible to reduce the input scale noise by that amount when at the lowest receiving level.

[0022] Furthermore, in the aforementioned example, an N-channel MOS-type FET serving as a variable impedance element was used, but the present invention is not limited thereto, and of course, a P channel MOS-type FET can be used, as well as a bipolar transistor or other semiconductor element can be used as a variable impedance element.

[0023]

[Advantageous Effects of the Invention] It is clear from the above discussion that when the present invention preamplifier circuit for photoelectric conversion is used, an inverting amplifier circuit is constructed, utilizing a plurality of inverting amplifiers, with a variable impedance element connected to the input terminal and the output terminal of the inverting amplifier of the first stage of said multistage inverting amplifier circuit, and there is also provided an impedance control means that controls the impedance of said variable impedance element in response to an output signal of the inverting amplifier of the first stage of said inverting amplifier circuit constructed in multiple stages, and when the input signal increases, the impedance of said variable impedance element is controlled so that it decreases, with the result that there is much greater speed of response to changes in the input signal, making it possible to operate stably up to a high transmission bit rate, while ensuring a broad dynamic range.

[0024] Moreover, since the impedance of the aforementioned variable impedance element is set so that it is infinitely great at the lowest receiving level for the input signal, it is possible

to eliminate the effects of thermal noise of the variable impedance element when at the lowest receiving level, making it possible to reduce the input scale noise when at the lowest receiving level.

[Brief Description of the Drawings]

[FIG. 1] A circuit diagram of a present invention preamplifier circuit for photoelectric conversion.

[FIG. 2] A graph showing an example of the input and output characteristics of the impedance control amplifier in FIG. 1.

[FIG. 3] A graph showing an example of the impedance characteristics of the FET in FIG. 1.

[FIG. 4] A wave form analysis graph of pulse signal output generated by computer for the circuit of the present invention.

[FIG. 5] A circuit diagram showing the first example of a prior art preamplifier circuit for photoelectric conversion.

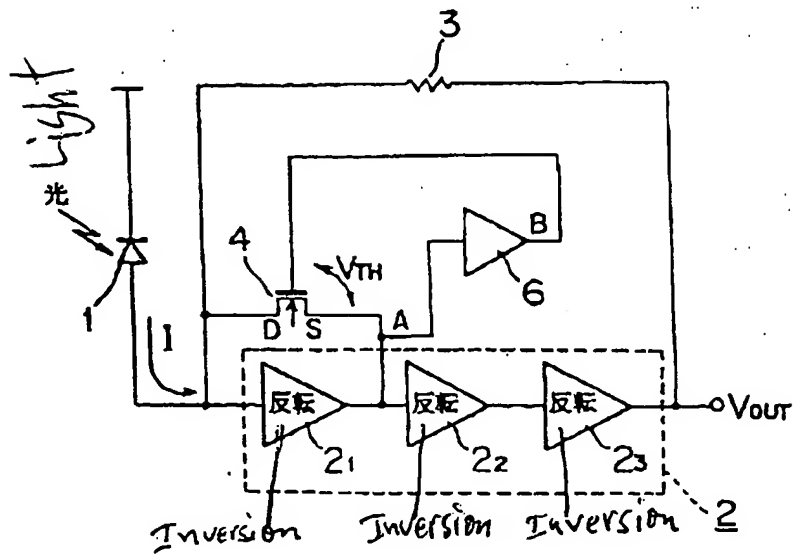
[FIG. 6] A circuit diagram showing the second example of a prior art preamplifier circuit for photoelectric conversion.

[Explanation of the Reference Numbers]

1 Photodiode (photoelectric conversion element)
2 Inverting amplifier circuit
2_1 - 2_3 Inverting amplifiers
3 Negative feedback resistor
4 FET (impedance variation element)
6 Impedance control amplifier (impedance control means)

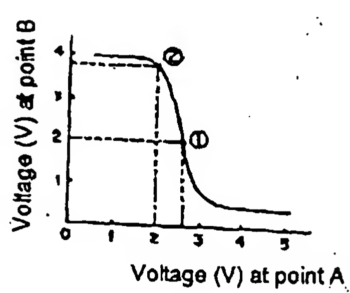
[FIG. 1]

Example



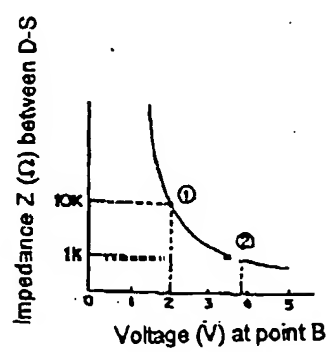
[FIG. 2]

Input and output characteristics of the impedance control amplifier in FIG. 1



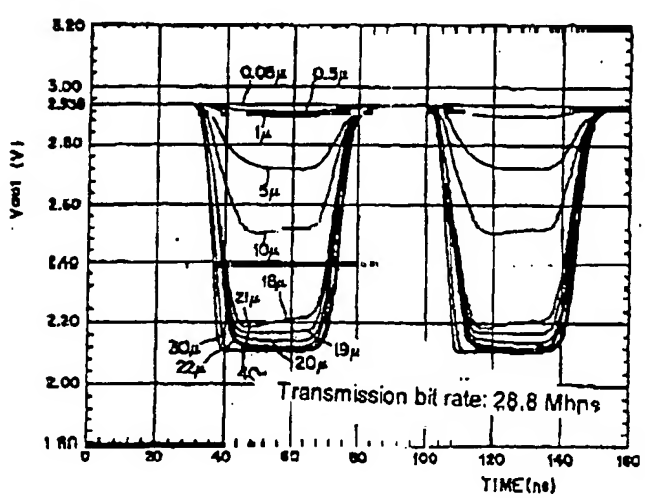
[FIG. 3]

Impedance characteristics of the FET



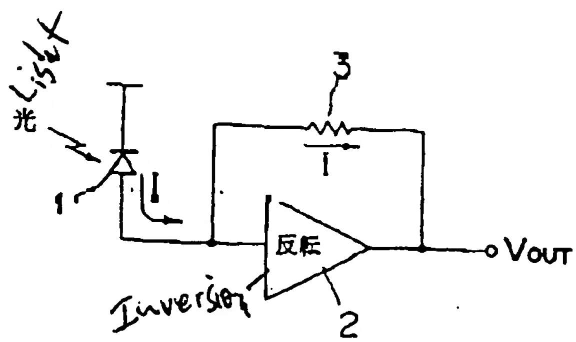
[FIG. 4]

A wave form analysis graph of pulse signal output generated by computer for the circuit of the present invention



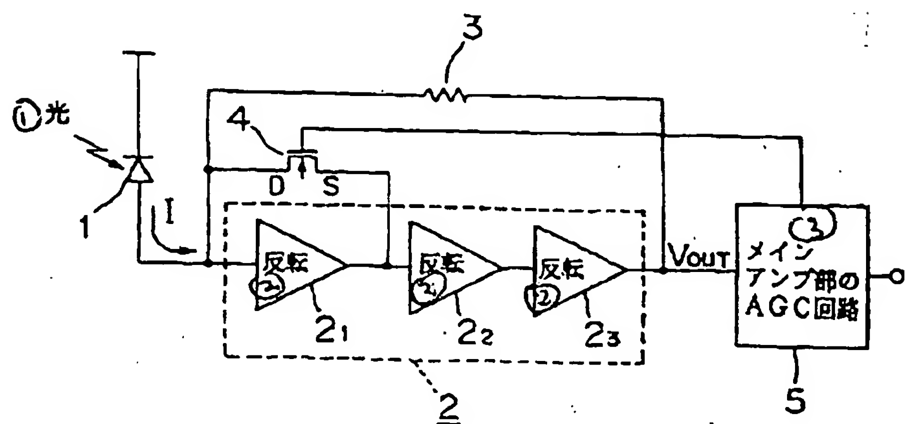
[FIG. 5]

The first example of a prior art preamplifier circuit for photoelectric conversion



[FIG. 6]

The second example of a prior art preamplifier circuit for photoelectric conversion



Key:

(1) Light
(2) Inversion
(3) AGC circuit of
the main amplifier part

Translated by John F. Bukacek (773/508-0352)

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最終頁に続く

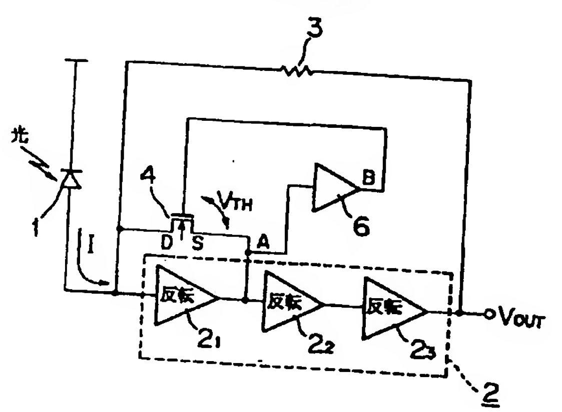
(54)【発明の名称】　光電変換用プリアンプ回路

(57)【要約】

【目的】　光通信における光伝送用受信器の入力段などに用いられる光電変換用プリアンプ回路に関し、広いダイナミックレンジを確保しながら高い伝送ビットレートまで安定に動作するプリアンプ回路を提供することを目的とする。

【構成】　光信号を電気信号に変換する光電変換素子と、該変換された電気信号を入力信号とし、入出力端子間に負帰還抵抗を接続された反転増幅回路とからなる光電変換用プリアンプ回路において、反転増幅回路を複数個の反転増幅器を用いて多段構成し、第一段目の反転増幅器の入出力端子間に可変インピーダンス素子を接続するとともに、多段構成した反転増幅回路の第一段目の反転増幅器の出力信号に応じて可変インピーダンス素子のインピーダンスを制御するインピーダンス制御手段を設け、入力信号が増加したとき可変インピーダンス素子のインピーダンスが小さくなるように制御するよう構成する。

実 施 例



1

【特許請求の範囲】

【請求項1】　光信号を電気信号に変換する光電変換素子と、該変換された電気信号を入力信号とし、入出力端子間に負帰還抵抗を接続された反転増幅回路とからなる光電変換用プリアンプ回路において、
前記反転増幅回路を複数個の反転増幅器を用いて多段構成し、
該多段構成した反転増幅回路の第一段目の反転増幅器の入出力端子間に可変インピーダンス素子を接続するとともに、
該多段構成した反転増幅回路の第一段目の反転増幅器の出力信号に応じて前記可変インピーダンス素子のインピーダンスを制御するインピーダンス制御手段を設け、
入力信号が増加したとき前記可変インピーダンス素子のインピーダンスが小さくなるように制御することを特徴とする光電変換用プリアンプ回路。

【請求項2】　入力信号の最小受信レベル時に可変インピーダンス素子のインピーダンスが無限大となるように設定し、最小受信レベル時の入力換算雑音を低減したことを特徴とする請求項1記載の光電変換用プリアンプ回路。

【請求項3】　可変インピーダンス素子がMOS型FETから構成されていることを特徴とする請求項1または2記載の光電変換用プリアンプ回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、光通信における光伝送用受信器の入力段などに用いられる光電変換用プリアンプ回路に関する。

【0002】

【従来の技術】図5に、従来の光伝送用受信器における光電変換用プリアンプ回路を示す。図5において、1は光パルス信号を受光して入力信号電流Ｉに変換するフォトダイオード、2は前記入力信号電流Ｉを増幅する反転増幅回路、3はこの反転増幅回路2の入出力端子間に接続された負帰還抵抗である。

【0003】図5の光電変換用プリアンプ回路は、トランスインピーダンス型プリアンプ回路と呼ばれるもので、その出力電圧V_{OUT}は、負帰還抵抗3の抵抗値をR_fとすると、$V_{OUT} = -(I \times R_f)$で与えられる。

【0004】ところで、光通信における光電変換用プリアンプ回路は、高速伝送を行なう必要から広いダイナミックレンジを必要とするが、図5の回路の場合、入力信号電流Ｉが大きくなり過ぎると、反転増幅回路2の出力電圧V_{OUT}が飽和してしまうため、出力パルスのデューティ比が変化してしまい、ダイナミックレンジをそれ以上に広く採れないという問題があった。

【0005】そこで、従来、このような問題を解決するため、負帰還抵抗3に流れ込む入力信号電流Ｉを分流し、反転増幅回路の飽和を防止する方法が採られていた。

2

【0006】図6にその回路構成を示す。図6において、1はフォトダイオード、2は三個の反転増幅器2_1～2_3によって多段構成された反転増幅回路、3は反転増幅回路2の入出力端子間を結ぶ負帰還抵抗、4は反転増幅回路2の第一段目の反転増幅器2_1の入出力端子間に接続された分流用の可変インピーダンス素子たるNチャンネルMOS型FET、5は光電変換用プリアンプ回路の後段に接続されたメインアンプ部の自動利得制御（AGC）回路である。

【0007】図6の光電変換用プリアンプ回路の場合、入力信号電流Ｉが増加して反転増幅回路2の出力電圧V_{OUT}が大きくなると、後段のメインアンプ部のAGC回路5によってFET4のゲート電圧を制御し、FET4のドレイン（D）－ソース（S）間のインピーダンスを下げることにより入力信号電流Ｉの一部をこのFET4へ分流し、これによって反転増幅回路2の飽和を防止したものである。

【0008】

【発明が解決しようとする課題】しかしながら、図6の光電変換用プリアンプ回路の場合、入力信号電流Ｉを分流するFET4は、後段のメインアンプ部のAGC回路5によって制御されているため、入力信号の変化に対する応答速度が遅く、広いダイナミックレンジを確保しながら高い伝送ビットレートまで安定に動作させることが難しいという問題があった。

【0009】本発明は、前記事情に基づきなされたもので、その目的とするところは、入力信号の変化に対する応答速度が速く、広いダイナミックレンジを確保しながら高い伝送ビットレートまで安定に動作できる光電変換用プリアンプ回路を提供することである。

【0010】

【課題を解決するための手段】本発明は、光信号を電気信号に変換する光電変換素子と、該変換された電気信号を入力信号とし、入出力端子間に負帰還抵抗を接続された反転増幅回路とからなる光電変換用プリアンプ回路において、前記反転増幅回路を複数個の反転増幅器を用いて多段構成し、前記多段構成した反転増幅回路の第一段目の反転増幅器の入出力端子間に可変インピーダンス素子を接続するとともに、該多段構成した反転増幅回路の第一段目の反転増幅器の出力信号に応じて前記可変インピーダンス素子のインピーダンスを制御するインピーダンス制御手段を設け、入力信号が増加したとき前記可変インピーダンス素子のインピーダンスが小さくなるように制御することを特徴とするものである。

【0011】

【作用】反転増幅回路への入力信号が増大すると、インピーダンス制御手段がこれを第一段目の反転増幅器の出力信号の変化から検出し、可変インピーダンス素子のインピーダンスが小さくなるように制御する。このため、

負帰還抵抗に流れ込む入力信号の一部がこのインピーダンス素子側へ分流され、反転増幅回路の飽和が防止される。このため、反転増幅回路の飽和によって出力パルスのデユーティ比が変化することがなくなる。

【0012】しかも、多段構成された反転増幅回路の第一段目の反転増幅器の出力信号を用いて可変インピーダンス素子のインピーダンスを制御しているため、入力信号電流の変化に対する応答速度が極めて速く、高い伝送ビットレートまで安定に動作する。

【0013】

【実施例】以下、図面を参照して本発明の実施例につき説明する。図1に本発明になる光電変換用プリアンプ回路の1実施例を示す。図1において、1はフォトダイオード、2は三個の反転増幅器2_1～2_3によって多段構成された反転増幅回路、3は反転増幅回路2の入出力端子間に接続された負帰還抵抗、4は第一段目の反転増幅器2_1の入出力端子間に接続された分流用の可変インピーダンス素子たるNチャンネルMOS型FET、6はインピーダンス制御用増幅器である。なお、図6の従来回路と同一の部分には同一の符号を付して示した。

【0014】本発明の光電変換用プリアンプ回路は、図1に示すように、多段構成された反転増幅回路2の第一段目の反転増幅器2_1の出力端にインピーダンス制御用増幅器6を接続し、このインピーダンス制御用増幅器6によってFET4のゲート電圧を制御するようにしたものである。

【0015】図1の回路の動作を、図2および図3を参照して説明する。なお、図2はインピーダンス制御用増幅器6の入出力特性を、図3はFET4のインピーダンス特性を示すものである。

【0016】入力信号電流Iが飽和領域以下の正常な動作範囲内にあり、この時のインピーダンス制御用増幅器6の動作点が図2中の①点であるものとすると、これに対応するFET4の動作点は図3中の①点となる。したがって、この場合におけるFET4のD－S間インピーダンスZは、例えば図3中に示すように、10KΩ程度の大きな値となっている。

【0017】いま、入力信号電流Iが増大し、FET4に流れる電流が増加すると、インピーダンス制御用増幅器6の入力端Aの電位は図2の①点から②点のように変化し、出力端Bの電位が大きくなる。これにより、FET4の動作点は図3の①点から②点のように変化し、FET4のD－S間インピーダンスZは、例えば図3中に示すように、10KΩから1KΩへと大きく低下する。

【0018】このインピーダンス低下の結果、FET4への入力信号電流Iの分流分が増え、負帰還抵抗3へ流れ込む入力信号電流Iが減り、反転増幅回路2の出力電圧V_{OUT}がその分だけ軽減されるので、入力信号電流Iの増大による反転増幅回路2の飽和が防止される。

【0019】したがって、反転増幅回路2の飽和によって出力パルスのデユーティ比が変化することがなくなる。しかも、多段構成された反転増幅回路2の第一段目の反転増幅器2_1の出力信号を用いてFET4のインピーダンスを制御しているため、入力信号電流Iの変化に対する応答速度が極めて速く、高い伝送ビットレートまで安定に動作する。

【0020】図4に前記実施例による出力波形の計算機による解析結果例を示す。この図4は、伝送ビットレート28．8Mbpsのパルス信号を入力信号とし、この入力パルスの電流値を種々変えたときの反転増幅回路2の出力パルス波形を計算機を用いて解析したものである。図4から明らかなように、入力パルスの電流値が変化しても出力パルス波形の立ち上がり位置と立ち下がり位置は一定であり、デューティ比が一定に保たれていることが分かる。

【0021】なお、前記実施例において、入力信号電流Iが最小受信レベル時におけるインピーダンス制御用増幅器6の出力電圧が、FET4のゲートのスレッショルド電圧V_{TH}よりも小さくなるように設定しておけば、入力信号電流Iの最小受信レベル時にはFET4を遮断状態（インピーダンス無限大）とすることができ、最小受信レベル時のFET4のサーマルノイズの影響を排除することができ、その分だけ最小受信レベル時の入力換算雑音を低減することができる。

【0022】また、前記実施例では、可変インピーダンス素子としてNチャンネルMOS型FETを用いたが、これに限らず、PチャンネルMOS型FET、さらには、バイポーラ・トランジスタなど、他の半導体素子を可変インピーダンス素子として用い得ることは当然である。

【0023】

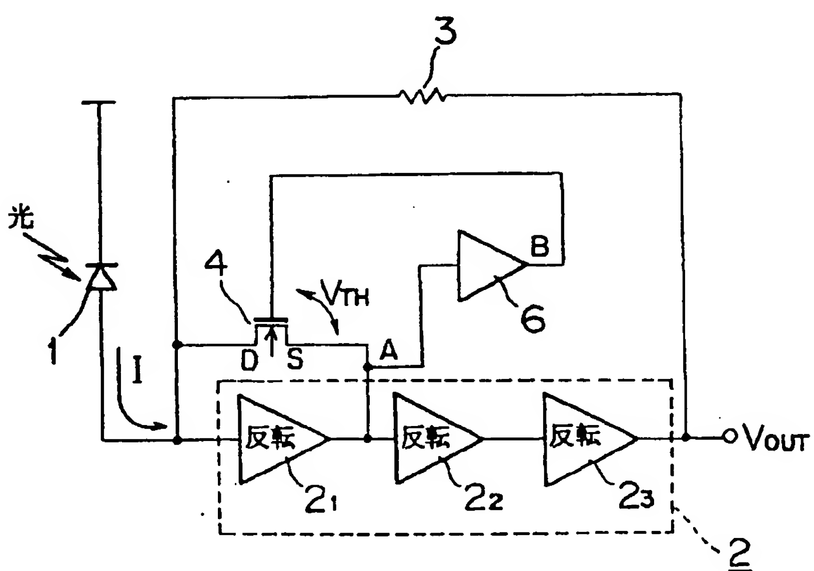
【発明の効果】以上述べたところから明らかなように、本発明の光電変換用プリアンプ回路によるときは、反転増幅回路を複数個の反転増幅器を用いて多段構成し、該多段構成した反転増幅回路の第一段目の反転増幅器の入出力端子間に可変インピーダンス素子を接続するとともに、該多段構成した反転増幅回路の第一段目の反転増幅器の出力信号に応じて前記可変インピーダンス素子のインピーダンスを制御するインピーダンス制御手段を設け、入力信号が増加したとき前記可変インピーダンス素子のインピーダンスが小さくなるように制御するようにしたので、入力信号の変化に対する応答速度が極めて速くなり、広いダイナミックレンジを確保しながら高い伝送ビットレートまで安定に動作させることができる。

【0024】また、入力信号の最小受信レベル時に前記可変インピーダンス素子のインピーダンスが無限大となるように設定したので、最小受信レベル時の可変インピーダンス素子のサーマルノイズの影響を排除することができ、最小受信レベル時の入力換算雑音を低減することができる。

【図面の簡単な説明】
【図1】本発明になる光電変換用プリアンプ回路の1実施例の回路図である。
【図2】図1中のインピーダンス制御用増幅器の入出力特性の一例を示す図である。
【図3】図1中のFETのインピーダンス特性の1例を示す図である。
【図4】本発明回路によるパルス信号出力の計算機による解析波形図である。
【図5】従来の光電変換用プリアンプ回路の第1の例を示す回路図である。
【図6】従来の光電変換用プリアンプ回路の第2の例を示す回路図である。
【符号の説明】
1　フォトダイオード（光電変換素子）
2　反転増幅回路
2_1 ～2_3　反転増幅器
3　負帰還抵抗
4　FET（インピーダンス可変素子）
6　インピーダンス制御用増幅器（インピーダンス制御手段）

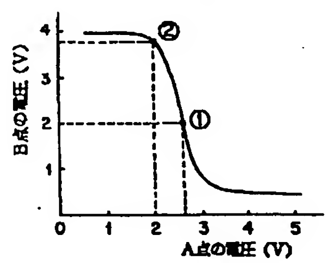
【図1】

実施例



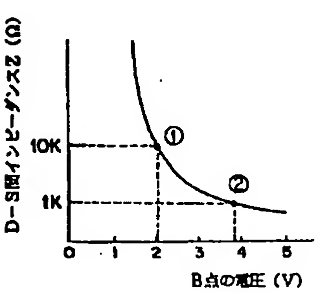
【図2】

インピーダンス制御用増幅器の入出力特性



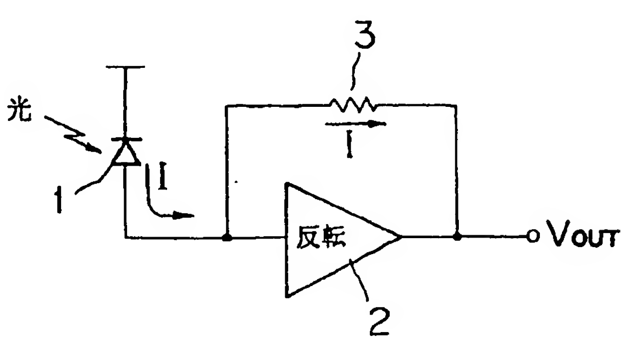
【図3】

FETのインピーダンス特性



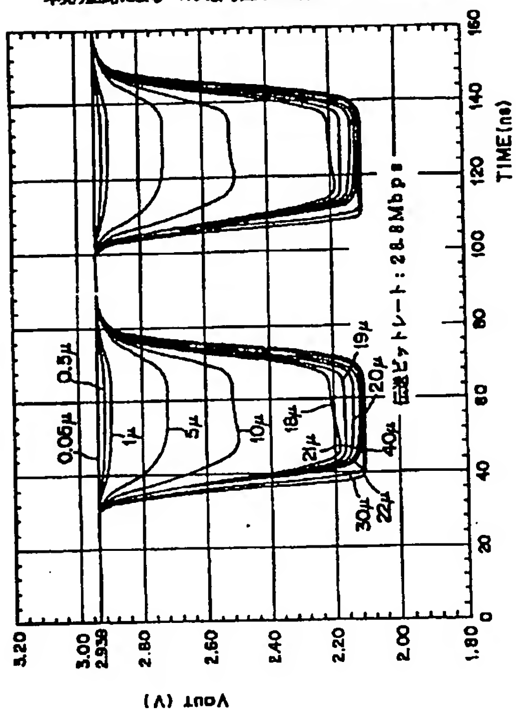
【図5】

従来の光電変換用プリアンプ回路の第1の例



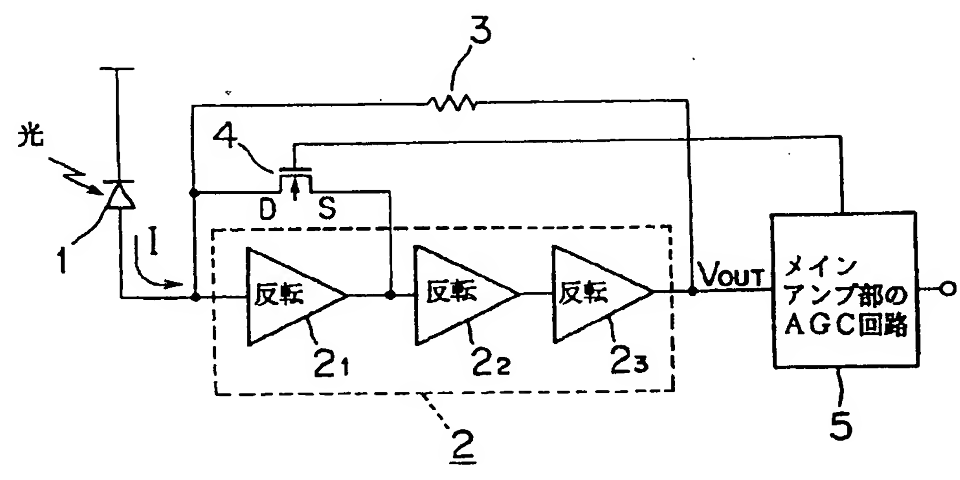
【図4】

本発明回路によるパルス信号出力の計算値による解析波形図



【図6】

従来の光電変換用プリアンプ回路の第2の例



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US-CL-CURRENT: 330/308

ABSTRACT:

PURPOSE: To provide a preamplifier circuit operated stably up to a high
transmission bit rate while securing a wide dynamic range with respect to a
photoelectric conversion preamplifier circuit used for an input stage or the
like of an optical transmitter/receiver in the optical communication.

CONSTITUTION: In the photoelectric conversion preamplifier circuit comprising a
photoelectric conversion element 1 converting an optical signal into an
electric signal and an inverting amplifier circuit 2

receiving the converted electric signal as an input signal and whose input terminal and output terminal are connected to a negative feedback resistor 3, the inverter amplifier circuit 2 is formed as a multi-stage by employing plural inverter amplifiers 2<SB>1</SB>-2<SB>3</SB>, a variable impedance element 4 is connected between the input output terminals of the 1st stage inverter amplifier 2<SB>1</SB>, an impedance control means 6 is provided, which controls an impedance of a variable impedance element 4 in response to an output signal of the 1st stage inverter amplifier 2<SB>1</SB> in the inverter amplifier circuit 2 of multi-stage configuration and when the input signal increases, the variable impedance element 4 is controlled so that its impedance is decreased.

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the preamplifier circuit for photo electric translation used for the input stage of the receiver for optical transmissions in optical communication etc.
[0002]
[Description of the Prior Art] The preamplifier circuit for photo electric translation in the conventional receiver for optical transmissions is shown in drawing 5 . In drawing 5 , the photodiode which 1 receives an optical pulse signal and is changed into input signal current I, the reversal amplifying circuit to which 2 amplifies the aforementioned input signal current I, and 3 are the negative feedback resistance connected between the input/output terminals of this reversal amplifying circuit 2.
[0003] It is called a transimpedance type preamplifier circuit and the preamplifier circuit for photo electric translation of drawing 5 is the output voltage VOUT. It is Rf about the resistance of the negative feedback resistance 3. If it carries out, it will be given by VOUT =- (IxRf).
[0004] By the way, the preamplifier circuit for photo electric translation in optical communication is the output voltage VOUT of the reversal amplifying circuit 2, if input signal current I becomes large too much in the case of the circuit of drawing 5 , although a latus dynamic range is needed from the need of performing high-speed transmission. Since it was saturated, the duty ratio of an output pulse changed and there was a problem that a dynamic range could not be taken more widely than it.
[0005] Then, in order to solve such a problem conventionally, the input signal current I which flows into the negative feedback resistance 3 was shunted, and the method of preventing the saturation of a reversal amplifying circuit was taken.
[0006] The circuitry is shown in drawing 6 . Setting to drawing 6 , 1 is a photodiode and 2 is three inverting amplifiers 21-23. The reversal amplifying circuit by which multi-stage composition was carried out, the negative feedback resistance whose 3 connects between the input/output terminals of the reversal amplifying circuit 2, and 4 are the inverting amplifier 21 of the first-stage eye of the reversal amplifying circuit 2. The N adjustable impedance-component slack MOSFET of part appropriation connected between input/output terminals and 5 are the automatic-gain-control (AGC) circuits of the main-amplifier section connected to the latter part of the preamplifier circuit for photo electric translation.
[0007] In the case of the preamplifier circuit for photo electric translation of drawing 6 , input signal current I increases and it is the output voltage VOUT of the reversal amplifying circuit 2. If it becomes large, the gate voltage of FET4 is controlled by AGC circuit 5 of the latter main-amplifier section, by lowering the impedance between the (Drain D)-sources (S) of FET4, a part of input signal current I will be shunted to this FET4, and the saturation of the reversal amplifying circuit 2 will be prevented by this.
[0008]
[Problem(s) to be Solved by the Invention] However, since FET4 which carries out diverging of the input signal current I was controlled by AGC circuit 5 of the latter main-amplifier section in the case of the preamplifier circuit for photo electric translation of drawing 6 , while the speed of response to

change of an input signal was slow and secured the latus dynamic range, there was a problem that it was difficult to operate stability to a high transmission bit rate.
[0009] It is offering the preamplifier circuit for photo electric translation which can operate to stability to a high transmission bit rate, the place which this invention was made based on the aforementioned situation, and is made into the purpose having a quick speed of response to change of an input signal, and securing a latus dynamic range.
[0010]
[Means for Solving the Problem] In the preamplifier circuit for photo electric translation which consists of a reversal amplifying circuit to which this invention made the input signal the optoelectric transducer which changes a lightwave signal into an electrical signal, and the this changed electrical signal, and negative feedback resistance was connected between input/output terminals While carrying out multi-stage composition of the aforementioned reversal amplifying circuit using two or more inverting amplifiers and connecting an adjustable impedance component between the input/output terminals of the inverting amplifier of the first-stage eye of the reversal amplifying circuit which carried out [aforementioned] multi-stage composition.The impedance control means which control the impedance of the aforementioned adjustable impedance component according to the output signal of the inverting amplifier of the first-stage eye of this reversal amplifying circuit that carried out multi-stage composition are prepared. When an input signal increases, it is characterized by controlling so that the impedance of the aforementioned adjustable impedance component becomes small.
[0011]
[Function] If the input signal to a reversal amplifying circuit increases, impedance control means will detect this from change of the output signal of the inverting amplifier of a first-stage eye, and it will control so that the impedance of an adjustable impedance component becomes small. For this reason, a part of input signal which flows into negative feedback resistance is shunted to this impedance-component side, and the saturation of a reversal amplifying circuit is prevented. For this reason, it is lost that the duty ratio of an output pulse changes with the saturation of a reversal amplifying circuit.
[0012] And since the impedance of an adjustable impedance component is controlled using the output signal of the inverting amplifier of the first-stage eye of the reversal amplifying circuit by which multi-stage composition was carried out, the speed of response to change of input signal current is very quick, and operates to stability to a high transmission bit rate.
[0013]
[Example] Hereafter, with reference to a drawing, it explains per example of this invention. One example of the preamplifier circuit for photo electric translation which becomes this invention at drawing 1 is shown. Setting to drawing 1 , 1 is a photodiode and 2 is three inverting amplifiers 21-23. The reversal amplifying circuit by which multi-stage composition was carried out, the negative feedback resistance to which 3 was connected between the input/output terminals of the reversal amplifying circuit 2, and 4 are the inverting amplifier 21 of a first-stage eye. The N adjustable impedance-component slack MOSFET of part appropriation connected between input/output terminals and 6 are the amplifier for impedance control. In addition, the same sign was attached and shown in the same portion as the conventional circuit of drawing 6 .
[0014] The preamplifier circuit for photo electric translation of this invention is the inverting amplifier 21 of the first-stage eye of the reversal amplifying circuit 2 by which multi-stage composition was carried out as shown in drawing 1 . The amplifier 6 for impedance control is connected to an outgoing end, and the gate voltage of FET4 is controlled by this amplifier 6 for impedance control.
[0015] Operation of the circuit of drawing 1 is explained with reference to drawing 2 and drawing 3 . In addition, drawing 2 shows the input-output behavioral characteristics of the amplifier 6 for impedance control, and drawing 3 shows the impedance characteristic of FET4.
[0016] Input signal current I is in a normal operating range below a saturation region, and if the operating point of the amplifier 6 for impedance control at this time shall be a ** point in drawing 2 , the operating point of FET4 corresponding to this will turn into ** point in drawing 3 . Therefore, the impedance Z between D-S of FET4 in this case serves as an about [10Kohm] big value, as shown for

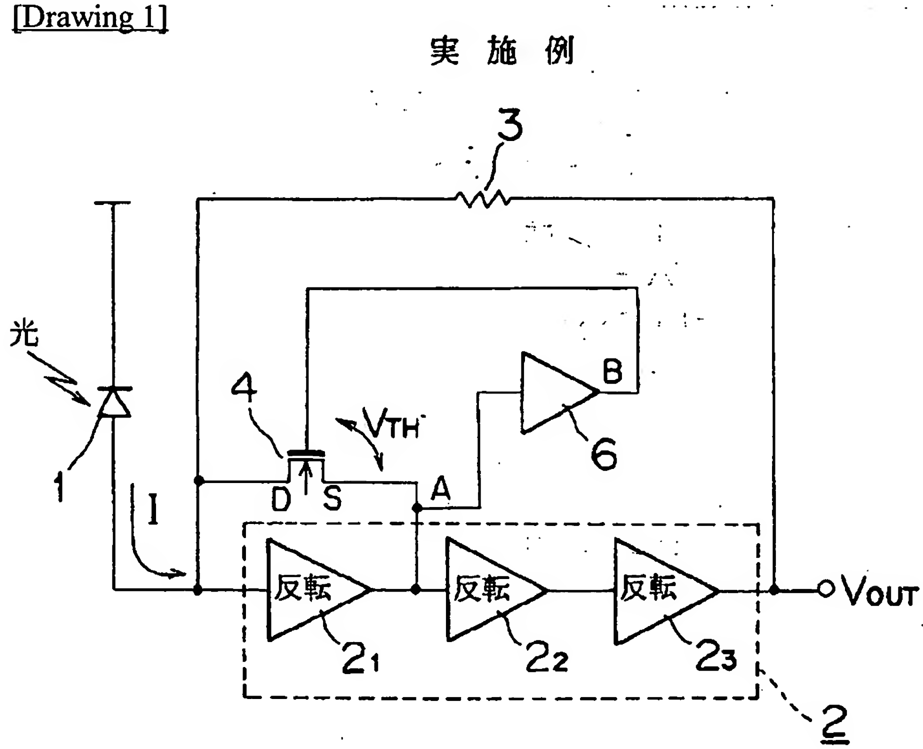
example, in drawing 3 .
[0017] Now, input signal current I increases, if the current which flows to FET4 increases, the potential of the input edge A of the amplifier 6 for impedance control will change like ** point to ** point of drawing 2 , and the potential of an outgoing end B will become large. Thereby, the operating point of FET4 changes like ** point to ** point of drawing 3 , and as the impedance Z between D-S of FET4 is shown for example, in drawing 3 , it falls from 10Kohm greatly to 1Komega.
[0018] As a result of this impedance fall, the amount of [of the input signal current I to FET4] diverging increases, the input signal current I which flows into the negative feedback resistance 3 decreases, and it is the output voltage VOUT of the reversal amplifying circuit 2. Since only the part is mitigated, the saturation of the reversal amplifying circuit 2 by increase of input signal current I is prevented.
[0019] Therefore, it is lost that the duty ratio of an output pulse changes with the saturation of the reversal amplifying circuit 2. And inverting amplifier 21 of the first-stage eye of the reversal amplifying circuit 2 by which multi-stage composition was carried out Since the impedance of FET4 is controlled using an output signal, the speed of response to change of input signal current I is very quick, and operates to stability to a high transmission bit rate.
[0020] The example of an analysis result by the computer of the output wave by the aforementioned example is shown in drawing 4 . This drawing 4 makes an input signal the pulse signal of transmission bit rate 28.8Mbps, and analyzes the output pulse wave of the reversal amplifying circuit 2 when changing various current value of this input pulse using a computer. Even if the current value of an input pulse changes so that clearly from drawing 4 , it falls with the standup position of an output pulse wave, and the position is fixed and it turns out that the duty ratio is kept constant.
[0021] In addition, if it sets up so that it may set in the aforementioned example and input signal current I may become [the output voltage of the amplifier 6 for impedance control at the time of the minimum receiving level] smaller than the threshold voltage VTH of the gate of FET4 FET4 can be made into a cut off state (impedance infinity) at the time of the minimum receiving level of input signal current I, the influence of the thermal noise of FET4 at the time of the minimum receiving level can be eliminated, and only the part can reduce the input conversion noise at the time of the minimum receiving level.
[0022] Moreover, although the N channel MOSFET was used as an adjustable impedance component in the aforementioned example, not only this but naturally it can use [a P channel MOSFET and] other semiconductor devices, such as a bipolar transistor, as an adjustable impedance component further.
[0023]
[Effect of the Invention] When calling at the preamplifier circuit for photo electric translation of this invention so that clearly from the place described above While carrying out multi-stage composition of the reversal amplifying circuit using two or more inverting amplifiers and connecting an adjustable impedance component between the input/output terminals of the inverting amplifier of the first-stage eye of this reversal amplifying circuit that carried out multi-stage composition The impedance control means which control the impedance of the aforementioned adjustable impedance component according to the output signal of the inverting amplifier of the first-stage eye of this reversal amplifying circuit that carried out multi-stage composition are prepared. Since it was made to control so that the impedance of the aforementioned adjustable impedance component becomes small when an input signal increased While the speed of response to change of an input signal becomes very quick and secures a latus dynamic range, stability can be operated to a high transmission bit rate.
[0024] Moreover, since it set up so that the impedance of the aforementioned adjustable impedance component might become infinite at the time of the minimum receiving level of an input signal, the influence of the thermal noise of the adjustable impedance component at the time of the minimum receiving level can be eliminated, and the input conversion noise at the time of the minimum receiving level can be reduced.

[Translation done.]

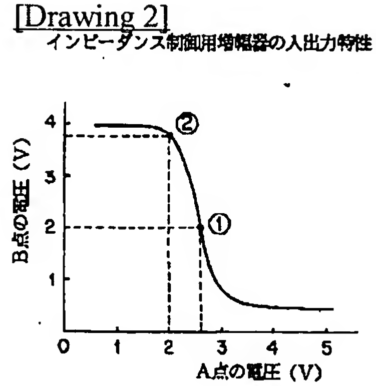
* NOTICES *

DRAWINGS

[Drawing 1]

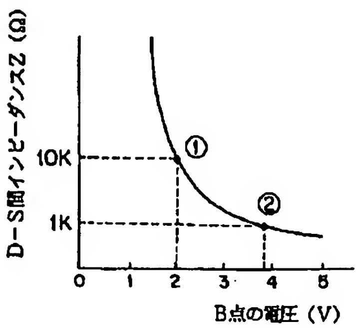


[Drawing 2]

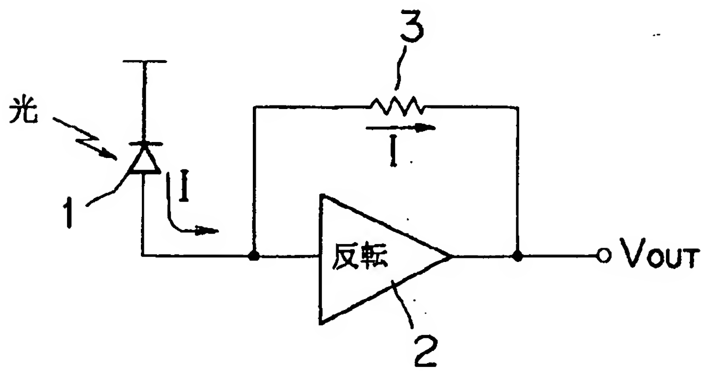


[Drawing 3]

FETのインピーダンス特性

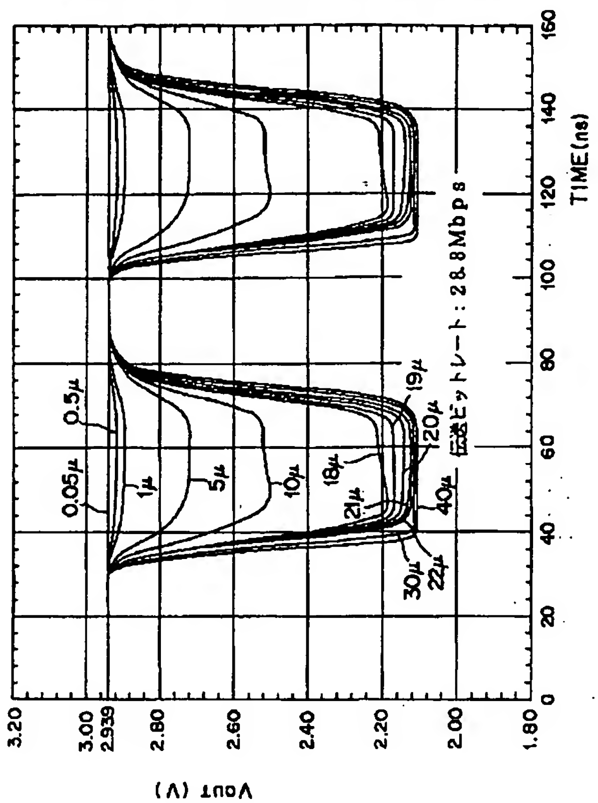


[Drawing 5]
従来の光電変換用プリアンプ回路の第１の例



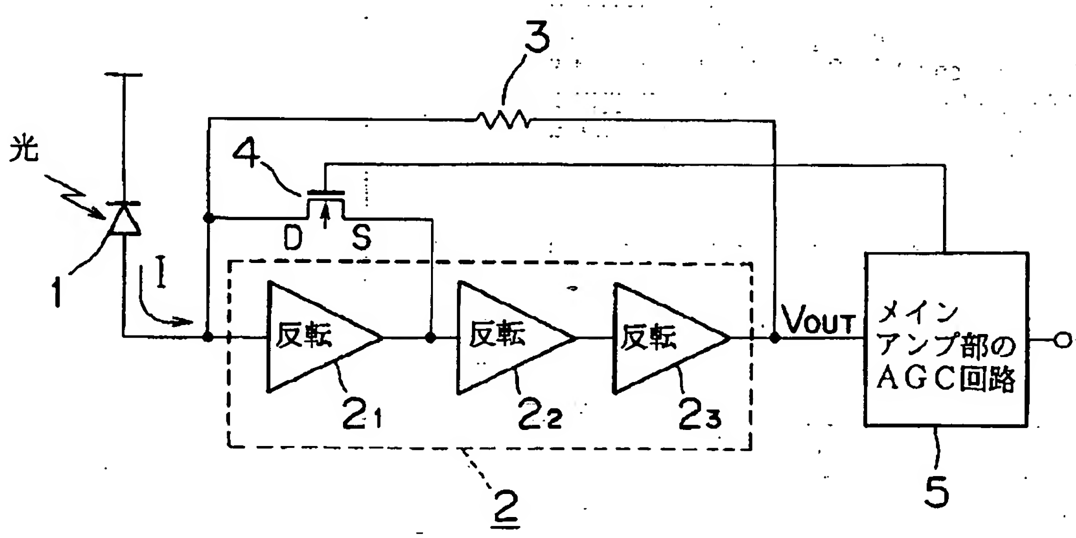
[Drawing 4]

本発明回路によるパルス信号出力の計算機による解析波形図



[Drawing 6]

従来の光電変換用プリアンプ回路の第２の例



[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram of one example of the preamplifier circuit for photo electric translation which becomes this invention.
[Drawing 2] It is drawing showing an example of the input-output behavioral characteristics of the amplifier for impedance control in drawing 1 .
[Drawing 3] It is drawing showing one example of the impedance characteristic of FET in drawing 1 .
[Drawing 4] It is an analysis wave form chart by the computer of the pulse signal output by this invention circuit.
[Drawing 5] It is the circuit diagram showing the 1st example of the conventional preamplifier circuit for photo electric translation.
[Drawing 6] It is the circuit diagram showing the 2nd example of the conventional preamplifier circuit for photo electric translation.
[Description of Notations]
1 Photodiode (Optoelectric Transducer)
2 Reversal Amplifying Circuit
21 -23 Inverting Amplifier
3 Negative Feedback Resistance
4 FET (Impedance Adjustable Element)
6 Amplifier for Impedance Control (Impedance Control Means)

[Translation done.]

Docket#: **MP0426** **PATENT**

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, I, the undersigned,

Farbod Aram

who have created a certain invention for which an application for United States Letters Patent was executed by me concurrently herewith and entitled:

Variable-Gain Constant-Bandwidth Transimpedance Amplifier

Do hereby sell, assign and transfer to Marvell Semiconductor, Inc., a corporation of California, having a place of business at 700 First Avenue, Sunnyvale, California 94089, its successors, assigns, and legal representatives, the full and exclusive right to said invention and said application and to any and all inventions described in said application for the United States, its territorial possessions and all foreign countries, and the entire right, title and interest in and to any and all Letters Patent which may be granted therefor in the United States, its territorial possessions and all foreign countries; and in and to any and all continuations-in-part, continuations, divisions, substitutes, reissues, extensions thereof, and all other applications for Letters Patent relating thereto which have been or shall be filed in the United States, its territorial possessions and/or any foreign countries, and all rights, together with all priority rights, under any of the international conventions, unions, agreements, acts, and treaties, including all future conventions, unions, agreements, acts, and treaties;

Agree that Marvell Semiconductor, Inc., hereinafter referred to as Assignee, may apply for and receive Letters Patent for said invention and said inventions, hereinafter referred to as said invention, in its own name, in the United States, its territorial possessions, and all foreign countries; and that, when requested to carry out in good faith the intent and purpose of this assignment, at the expense of said Assignee, its successors, assigns and legal representatives, the undersigned will execute all continuations-in-part, continuations, divisions, substitutes, reissues, extensions thereof, execute all rightful oaths, assignments, powers of attorney and other papers, testify in any legal or quasi legal proceedings; communicate to said Assignee, its successors, assigns or legal representatives all facts known to the undersigned relating to said invention and the history thereof; and generally do everything possible which said Assignee, its successors, assigns, or legal representatives shall consider desirable for aiding in securing, maintaining and enforcing proper patent protection for said invention and for vesting title to said invention and all applications for patents on said invention in said Assignee, its successors, assigns, or legal representatives; and

Covenant with said Assignee, its successors, assigns, or legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

IN TESTIMONY WHEREOF I have hereunto set MY signature on the date indicated below.

Full Name of Sole/First Inventor: Farbod Aram	
Inventor's Signature:	Date: Month/Day/Year 3/30/04

Form Letters1